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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/692,803	10/27/2003	Hsin-Hung Chen	CHEN3593/EM	9676

23364 7590 02/01/2007

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EXAMINER	
DO, CHAT C	
ART UNIT	**PAPER NUMBER**
2193	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/01/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/692,803	CHEN ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/27/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 1 is objected to because of the following informalities:

Re claim 1, the applicant is advised to rewrite the word "signalse" in line 16 as "signals" for clarification.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-15 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1-15 cites a method for transforming a function in hardware according to a mathematical algorithm. In order for claims to be statutory, claims must either include a practical application or a concrete, useful, and tangible result. However, claims 1-15 just merely disclose steps of arranging and computing the transformation in hardware without further disclosing a practical application or tangible result for the transformation.

Therefore, claims 1-15 are directed to non-statutory subject matter.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-8 and 10-15 are rejected under 35 U.S.C. 103(a) as being obvious over Chi-Li et al. ("An improved time-recursive lattice structure for low-latency IFFT architecture in DMT transmitter") in view of Richard ("Subexprssion sharing in filters using canonic signed digit multipliers").

Re claim 1, Chi-Li et al. discloses in Figures 1-2 and 7 a method of constructing a hardware architecture for transform functions (e.g. abstract lines 1-3 page IV-250), comprising the steps of: a setting-up step of a transform function, to select a transform function which transfers an input signal x(n) on a domain into an output signal y(k) on another domain (e.g. right column of page IV-250 as theoretical analysis); a simplifying step processed by a fixed-one-input multiplier (e.g. Figure 1 as lattice module multiplier and Figure 7 with section 4 "fixed-point analysis"); a multiplying step (e.g. under the module array in Figure 2), to separately use the fixed-one-input multipliers for multiplying the input signals by the value-specific transform coefficients and generating the intermediate results (e.g. output of the module array and paragraph right under the caption of Figure 1); a distributing step, to use a path-selector to distribute the product results to accumulators according to the timing diagrams of the output signals (e.g. expanding circuit in Figure 2 for routing the intermediate products to appropriated

accumulators); an accumulating step, to use the accumulators to perform the accumulations at the correct timing diagrams to generate the accumulated results (e.g. adder and register with feedback as accumulators in Figure 2); a constant multiplying step, to use the multipliers to multiply the accumulated results by a constant-value item of the transform function and generate the output signals (e.g. shift right by log2(N) in Figure 2); and an outputting step, to output the output signals (e.g. yield the output of transformed x(0) to x(2N-1). Chi-Li et al. fail to disclose the step to simplify each group of transform coefficients with the same value as an identical transform coefficient, wherein every identical transform coefficient is respectively. However, Richard discloses in Figure 1 the step of to simplify each group of transform coefficients with the same value as an identical transform coefficient, wherein every identical transform coefficient is respectively as CSD format (e.g. under the section I "Canonic signed digit multiplication"). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the step to simplify each group of transform coefficients with the same value as an identical transform coefficient, wherein every identical transform coefficient is respectively as seen in Richard's invention into Chi-Li et al.'s invention because it would enable to increase dramatically the overall performance by sharing the common subexpressions (e.g. abstract).

Re claim 2, Chi-Li et al. further discloses in Figures 1-2 and 7 the transform function is y(k) = A sum(T(k,n)x(n)) for k=0,1,2, . . . , N-1, where A is the constant item and T.sub.c(k,n) is the corresponding transform coefficient (e.g. expression 3 in page IV-250 right column).

Re claim 3, Chi-Li et al. further discloses in Figures 1-2 and 7 the transform function is applied to perform an inverse discrete Fourier transform (IDFT) for A = 1/N (e.g. expression 6 in page IV-250 right column with N as 2N).

Re claim 4, Chi-Li et al. further discloses in Figures 1-2 and 7 a simplifying step of symmetry-based transform coefficients after the simplifying step of transform coefficients to simplify symmetric transform coefficients for sharing a fixed-one-input multiplier (e.g. section 3 and sections 3.1 in page IV-251).

Re claims 5-6, Chi-Li et al. fail to disclose in Figures 1-2 and 7 the transform coefficients are represented in a binary form and further each of the fixed-one-input multipliers respectively computes the corresponding transform coefficient consists of at least one addition or subtraction unit. However, Richard discloses in Figures 1-2 the transform coefficients are represented in a binary form (e.g. under the notation in the left column) and further each of the fixed-one-input multipliers respectively computes the corresponding transform coefficient consists of at least one addition or subtraction unit (e.g. under section I "Canonic signed digit multiplication", particularly Figure 2). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the step of the transform coefficients are represented in a binary form and further each of the fixed-one-input multipliers respectively computes the corresponding transform coefficient consists of at least one addition or subtraction unit as seen in Richard's invention into Chi-Li et al.'s invention because it would enable to increase dramatically the overall performance by sharing the common subexpressions (e.g. abstract).

Re claims 7-8, Chi-Li et al. fail to disclose in Figures 1-2 and 7 the multiplying step comprises the steps of: determining values of all transform coefficients; analyzing the bit values of transform coefficients for extracting shared items, wherein each shared item is calculated by the addition and/or subtraction units; and trying to construct the values of transform coefficients by using the shared items and further the transform coefficients are represented by a canonic signed digit (CSD). However, Richard discloses in Figures 1-2 the multiplying step comprises the steps of: determining values of all transform coefficients; analyzing the bit values of transform coefficients for extracting shared items, wherein each shared item is calculated by the addition and/or subtraction units; and trying to construct the values of transform coefficients by using the shared items and further the transform coefficients are represented by a canonic signed digit (e.g. under section I "Canonic signed digit multiplication", particularly Figure 2). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the step of the multiplying step comprises the steps of determining values of all transform coefficients; analyzing the bit values of transform coefficients for extracting shared items, wherein each shared item is calculated by the addition and/or subtraction units; and trying to construct the values of transform coefficients by using the shared items and further the transform coefficients are represented by a canonic signed digit as seen in Richard's invention into Chi-Li et al.'s invention because it would enable to increase dramatically the overall performance by sharing the common subexpressions (e.g. abstract).

Re claim 9, Chi-Li et al. further discloses in Figures 1-2 and 7 the transform coefficients are represented by a hybrid signed digit (HSD).

Re claim 10, it is an apparatus claim of claim 1. Thus, claim 10 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 11, it is an apparatus claim of claim 1. Thus, claim 11 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 12, it is an apparatus claim of claim 2. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 13, it is an apparatus claim of claim 5. Thus, claim 13 is also rejected under the same rationale as cited in the rejection of rejected claim 5.

Re claim 14, it is an apparatus claim of claim 6. Thus, claim 14 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 15, Chi-Li et al. further discloses in Figures 1-2 and 7 the path-selector further comprises a controller to generate the control signals (e.g. inherently for selectively controlling the muxes in Figure 2).

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being obvious over Chi-Li et al. ("An improved time-recursive lattice structure for low-latency IFFT architecture in DMT transmitter") in view of Richard ("Subexprssion sharing in filters using canonic signed digit multipliers"), as applied to claim 7, in further view of Dhananjay et al. ("Hybrid signed-digit number systems: A unified framework for redundant number representations with bounded carry propagation chains").

Re claim 9, Chi-Li et al. in view of Richard fail to disclose in Figures 1-2 and 7 the transform coefficients are represented by a hybrid signed digit (HSD). However, the hybrid signed digit system is well-known in the art and widely used in many practical engineering applications as seen in Dhananjay et al. wherein Dhananjay et al. disclose the hybrid signed digit system under section III as hybrid number representation. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the HSD coefficients as seen in Dhananjay et al.'s invention into Chi-Li et al. in view of Richard's invention because it would enable to yield faster and compact adder and multiplier realizations (e.g. second and third paragraphs in the right column page 889).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 4,138,730 to Ali discloses a high speed FFT processor.

b. U.S. Patent No. 4,965,761 to Schlunt discloses a fast discrete fourier transform apparatus and method.

c. U.S. Patent No. 4,791,598 to Liou et al. disclose two-dimensional discrete cosine transform processor.

d. U.S. Patent No. 4,999,799 to Tufts discloses a signal processing apparatus for generating a fourier transform.

e. U.S. Patent No. 6,260,053 to Maulik et al. disclose an efficient and scalable FIR filter architecture for decimation.

f. U.S. Patent No. 6,757,326 to Prieto et al. disclose a method and apparatus for implementing wavelet filters in a digital system.

g. U.S. Patent No. 6,041,340 to Mintzer discloses a method for configuring an FPGA for large FFTS and other vector rotation computations.

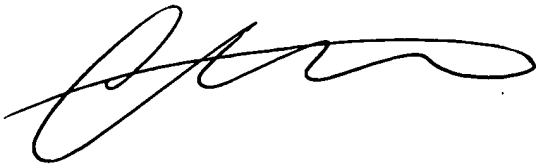
h. U.S. Patent Publication No. 2003/0212722 to Jain et al. disclose an architecture for performing fast fourier-type transforms.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193



January 29, 2007